METHOD AND DEVICE FOR SIGNALING A TRANSMISSION FAULT

ON A DATA LINE

5

Background of the Invention:

Field of the Invention:

For communications purposes, data links that use a high data
rate ("High-Speed data paths") are preferably configured using
10   differential signaling. The expression "differential
signaling" in this case refers to two signal conductors being
provided for the transmission of the data signals and are
operated with opposite polarity or in antiphase. The
standards TIA-LVDS and EIA-LVDS (LVDS: low voltage
15   differential signals/signaling) exist for standardization of
differential signaling.

Differential signaling allows smaller signal amplitudes and is
less susceptible to disturbances than signal-phase (signal-
20   ended) signaling in which only a single conductor is used for
the transmission of a data signal. Single-phase (signal-
ended) signaling is particularly suitable when there are a
very large number of signals or the signal density is very
high, but can be used only to a very restricted extent for the
25   transmission of high bit-rate signals. Owing to the fact that
the data rates are rising all the time, systems based on

differential signaling are thus becoming increasingly widely

used. Even complete bus systems are nowadays configured to

use differential signaling.

5   As the use of differential signaling increases in modern

electronic systems, there is an increasing requirement for the

capability to electronically test these systems during

manufacture before delivery, and in the field. One

particularly major aspect in this case is the testing of the

10   signal connections between the individual assemblies and

integrated circuits in a system. Even during manufacture,

there is an aim to identify at an early stage in particular

contact faults, such as short circuits between signal

conductors or to supply conductors, and unconnected (open)

15   signal conductors in order to make it possible to rework these

before further system integration, and to replace damaged

assemblies.

An electronic testing method for the identification of contact

20   faults has become increasingly widely used in recent years, in

which all the inputs and outputs of the components in the

system are connected to form a serial sampling register,

referred to as a boundary scan register.

25   This method has been standardized by the IEEE Computer Society

and has been published under the title "IEEE Standard Test

Access Port and Boundary-Scan Architecture" (IEEE Std.

1149.1). The test architecture specified by the IEEE Computer

Society is, however, suitable only for the evaluation of

single-phase signals and the identification of the contact

5   faults that may possibly occur on the signal conductors with

single-phase signals. However, it is not directly possible to

use the cited IEEE Standard with the aim of identifying all

possible contact faults when using differential signaling.

10   Summary of the Invention:

It is accordingly an object of the invention to provide a

method and a device for signaling a transmission fault on a

data line that overcome the above-mentioned disadvantages of

the prior art methods and devices of this general type, which

15   are suitable for identification of transmission faults when

using differential signaling.

With the foregoing and other objects in view there is

provided, in accordance with the invention, a method for

20   producing a fault signal indicating a fault in a transmission

of a data signal transmitted using differential signaling on a

data line having two signal lines. The method includes

comparing a first mid-level value having a potential in an

area of a mid-point between a signal level on a first signal

25   line and a signal level on a second signal line when

transmitting a logic "1" with a second mid-level value formed

when transmitting a logic "0". A fault signal is generated if a discrepancy between the first and second mid-level values exceeds a predetermined threshold value.

5   The invention provides for the evaluation of a mid-level signal, whose potential is in the area of the mid-point between the two signal levels on the two signal lines, in order to identify a fault. In this case, the expression signal level refers to the respective electrical potential,

10 that is to say the voltage potential on the signal conductors; the expression mid-level is the mean potential, that is to say, so to speak, the "mid-potential" whose potential is at the mid-point between the two potentials on the signal conductors. The invention in this case makes use of the

15 knowledge that when there is no disturbance to a data transmission, the mid-level signal or "mid-potential" between the two signal conductors remains unchanged even when the transmitted boundary information changes, that is to say even when switching takes place from a logic "1" to a logic "0", or

20 vice versa. If, on the other hand, there is a short circuit for example in one of the two signal conductors, for example a short to the ground potential, then the "mid-potential" or mid-level signal is shifted, and this can be used to identify a fault, and thus to produce a fault signal. One particularly

25 major advantage of the method according to the invention is in this case that it can be carried out very easily, specifically

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because only the mid-potential - that is to say only a single measurement variable - need be observed and evaluated; there is no need for any further measurement variables for the method according to the invention.

5

Particularly high measurement sensitivity for the method according to the invention is advantageously achieved if the evaluated mid-level signal or the evaluated mid-potential is exactly at the mid-point between two signal levels.

10   Specifically, this is achieved by producing the fault signal in accordance with the following "initiation condition":

$$| (VP[1] + VN[1])/2 - (VP[0] + VN[0])/2 | > Q \text{ or}$$
$$| (VP[0] + VN[0])/2 - (VP[1] + VN[1])/2 | > Q$$

15

The mathematical formula VP[1] denotes the signal level on the first signal line when a logic "1" is transmitted, VP[0] is the signal level on the first signal line when a logic "0" is transmitted, VN[1] is the signal level on the other signal

20   line when a logic "1" is transmitted, VN[0] is the signal level on the other signal line when a logic "0" is transmitted, and Q is the predetermined threshold value.

The tapping off or detection of the mid-level signals or mid-

25   potentials can be carried out particularly easily and this advantageously with the aid of a voltage divider which is

connected between the two signal lines; an ohmic-reactive

voltage divider can preferably be used in this case, with

identical resistors, in order that the mid-level signal is

tapped off as exactly as possible.

5

As already explained above, the signal level for the

transmission of a logic "0" and for the transmission of a

logic "1" are required for the method according to the

invention. Since these levels do not occur at the same time

10   or simultaneously, at least one signal level must be buffer-

stored. This can advantageously be done by using a sample and

hold device, and it is thus regarded as being advantageous for

at least one of the two mid-level signals to be buffer-stored

with the aid of a sample and hold device. This can

15   advantageously be done in particular in such a way that the

mid-potential when a logic "1" is transmitted is sampled using

a sample and hold device and is buffer-stored as an auxiliary

measurement variable, with the corresponding mid-potential

when the logic "0" is transmitted likewise being sampled and

20   being buffer-stored as another auxiliary measurement variable,

and the fault signal being produced when the magnitude of the

difference between the two auxiliary measurement variables is

greater than the predetermined threshold value. Furthermore,

it is regarded as being advantageous for two sample and hold

25   devices to be used for detection of the signal levels, the

first of which is used to detect the mid-level signal when a

logic "1" is being transmitted and the other sample and hold

device is used to detect the mid-level signal when a logic "0"

is being transmitted. The measurement variables that are

stored by the two sample and hold devices can then be used to

5   produce the fault signal. The association between the sample

and hold device and the logic information ("1" or "0") and the

associated signal level can in this case be produced in a

particularly simple manner if logic "zeros" and "ones" are

transmitted alternately at a predetermined clock frequency on

10   the data line, and if the two sample and hold devices which

are connected to the data line operate at half the clock

frequency and in opposite senses, that is to say phase-shifted

through 180°.

15   Halving the clock rate and shifting the phase through 180° can

be achieved in a particularly simple manner, and thus

advantageously, with the aid of a toggle flip-flop, to whose

input side a predetermined clock frequency is applied and

whose output side is connected to the two sample and hold

20   devices, to be precise in such a manner that one output signal

from the toggle flip-flop is used as the auxiliary clock

signal for the first sample and hold device, and the other

output signal from the toggle flip-flop is used as the further

auxiliary clock signal for the second sample and hold device.

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In order to evaluate the fault signal that is produced using the method according to the invention, it is regarded as being advantageous for the fault signal to be stored in a shift register. In this case, the fault signal can then be

5 subsequently processed in an analogous manner to the "IEEE Standard Test Access Port and Boundary-Scan Architecture" test procedure which was explained initially, all that is necessary to do this is for the shift register to essentially be a boundary scan register in accordance with IEEE Standard cited

10 above, or for a corresponding shift register to be used which is matched to the requirements of differential signaling.

Furthermore, the invention is based on the object of specifying an apparatus for producing a fault signal that is

15 suitable for identification of transmission faults when using differential signaling.

The independent apparatus claim provides for the apparatus to have a comparison device which compares a mid-level signal,

20 whose potential is in the area of the mid-point between the signal level on the first signal line and the signal level on the other signal line when a logic "1" is transmitted with the corresponding mid-level signal when a logic "0" is transmitted, and which produces a fault signal when the

25 discrepancy between the two mid-level signals is greater than a predetermined threshold value.

In the same way as the method according to the invention in this case the apparatus according to the invention makes use of the knowledge that the mid-level signal or the mid-

5   potential between the two signal conductors shifts in the event of a fault. Reference can therefore be made to the above statements relating to the method according to the invention.

10   Merely for the sake of completeness, it should be mentioned that a comparator can advantageously be used for the comparison of the two mid-level signals.

In order to avoid reflections of the data signal occurring at

15   the interface on the data line to the apparatus according to the invention, it is regarded as being advantageous for the input side of the apparatus to have a line termination which is connected to the data line and whose characteristic impedance is matched to that of the data line.

20

In addition, it is regarded as advantageous for the apparatus for storing and evaluating a fault situation to be followed by a shift register which is compatible with the boundary scan register as described in the IEEE Standard cited above; a

25   shift register such as this can be constructed in a simple and

thus advantageous manner by use of multiplexers and D-flip-flops.

Other features which are considered as characteristic for the

5   invention are set forth in the appended claims.

Although the invention is illustrated and described herein as embodied in a method and a device for signaling a transmission fault on a data line, it is nevertheless not intended to be

10 limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

15 The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

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Brief Description of the Drawings:

Fig. 1 is a block diagram of an exemplary embodiment of an apparatus according to the invention, which is suitable for carrying out the invention;

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Fig. 2 is a block diagram of an exemplary embodiment of a

comparison device, as can be used in the apparatus shown in

Fig. 1;

5   Fig. 3 is a block diagram of an exemplary embodiment of a

shift register that can be disposed downstream from the

comparison device shown in Fig. 2;

Fig. 4 is a graph showing an exemplary embodiment of a data

10 signal which is applied to the apparatus shown in Fig. 1

during operation without any faults; and

Fig. 5 is a graph showing an exemplary embodiment of a data

signal which is applied to the apparatus shown in Fig. 1 when

15 a fault is present.

Description of the Preferred Embodiments:

Referring now to the figures of the drawing in detail and

first, particularly, to Fig. 1 thereof, there is shown an

20 apparatus 5 for producing a fault signal F which indicates

that there is a transmission fault in the transmission of a

data signal D on a data line 10. The data line 10 shown in

Fig. 1 is formed by two signal lines 20 and 30 and is operated

using differential transmission techniques. Therefore, the

25 signal elements DIN[p] and DIN[n] which are transmitted on the

two signal lines 20 and 30 have a phase shift between them of 180° or π.

The first signal element DIN[p] on the one signal line 20 in
5 this case has two different signal levels, to be precise a signal level VP[1] for the transmission of a logic "1" and a signal level VP[0], which is not the same as VP[1], for the transmission of a logic "0".

10 A corresponding situation applies to the other signal element DIN[n], which likewise has two different signal levels. A signal level VN[1] is used for transmission of a logic "1" and a signal VN[0] which is not the same as VN[1], is used for transmission of a logic "0".
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The phase shift of 180° or π results in that, when there are no faults, the signal level VP[1] and VN[0] as well as the signal levels VP[0] and VN[1] are of the same magnitude. In the event of a fault, for example when a short circuit to
20 ground occurs, the signal levels change, however; for example in the event of a short circuit to ground, the faulty signal conductor is drawn to a signal level of 0 volts.

A line termination 40 is connected to the data line 10 and is
25 formed by two resistors RT as well as a resistor RB and a

capacitor CB for presetting and stabilizing a line connection voltage VB. The resistors RT are in this case chosen such that an input impedance of the apparatus 5 is matched to the characteristic impedance of the data line 10; normal

5   characteristic impedances are, for example 50 and 75 ohms.

A voltage divider 50 having two resistors RS (RS preferably has a high resistance in comparison to the line termination resistors RT) is connected to the data line 10 and these

10   resistors have the same resistance value. A potential which is exactly at the mid-point between the potential VP on the first signal line 20 and the potential VN on the other signal line 30 is thus produced at an output 60 of the voltage divider 50; in the following text, the potential is referred

15   to as the mid-potential or mid-level signal M. The value of the mid-level signal is calculated to be:

$$M = (VP[1] + VN[1])/2 \text{ for a logic "1"}$$

20   $$M = (VP[0] + VN[0])/2 \text{ for a logic "0".}$$

The mid-level signal is applied to a comparison device 70 whose output side produces a fault signal F when a transmission fault occurs. The method of operation of the

25   comparison device 70 will be explained further below in conjunction with Fig. 2.

In addition, the apparatus 5 also has an amplifier 80 for
signal processing. The two signal elements DIN[p] and DIN[n]
are applied to the input side of the amplifier 80. The

5 amplifier 80 uses these signal elements, for example, to
produce processed and amplified differential output data
signal Da[n] and Da[p] which are supplied to a "CML-CMOS"
conversion module 90 (CML: current mode logic) and to a
"Signal/Null-Detect" circuit 100. The conversion module 90

10 converts the differential output data signals Da[n] and Da[p]
to an output signal HSDIN which is suitable for transmission
on a single line and which is thus a single-ended signal. The
output signal HSDIN is in this case a CMOS-compatible signal.

15 The Signal/Null-Detect circuit 100 is formed by a comparison
module and emits as its output signal SD a logic "1" when
there is a sufficiently large voltage differential between the
two differential signal elements DIN[p] and DIN[n].
Conversely, a logic "0" is emitted when the input voltage

20 difference is too small. The Signal/Null-Detect circuit 100
in this case makes use of the fact that, with differential
signaling, there is always a voltage difference between the
two signal lines during data transmission, irrespective of
whether the logic "1" or a logic "0" is being transmitted.

25 The Signal/Null-Detect circuit 100 may, for example, be formed
by a comparator.

Furthermore, Fig. 1 shows a control line 110. The operating mode of the amplifier 80 can be switched via the control line 110 to be precise via a control signal INP_SEL which is

5   transmitted via the control line 110. The control signal INP_SEL also switches the line termination voltage between VP and VPP, to be precise via a switch 105.

Fig. 2 shows an exemplary embodiment of the comparison device

10   70 as shown in Fig. 1. This shows two sample and hold devices 200 and 210, to the respective inputs, E200 and E210, to both of which the mid-level signal M is applied. The two sample and hold devices 200 and 210 are each connected to a toggle flip-flop by their respective clock inputs T200 and T210 which

15   are edge-triggered and react to the rising edge. Specifically, a clock input T200 of the first sample and hold device 200 is connected to an output Q of the toggle flip-flop 220, and a clock input T210 of the other sample and hold device 210 is connected to the other output $\overline{Q}$ of the toggle

20   flip-flop 220. A clock signal TCK is applied on the input side of the toggle flip-flop 220, to be precise at an edge-triggered clock input T220 which reacts to the falling edge.

The two sample and hold devices 200 and 210 are each connected

25   on the output side to a comparison circuit 230.

The method of operation of the apparatus 5 shown in Fig. 1 will now be explained in conjunction with Figs. 2, 4 and 5.

5　In order to test the data line 10, the data signal D is transmitted via the data line 10. The date signal D contains a bit sequence, which alternates at a predetermined clock rate T and is composed of logic "zeros" and "ones"; the clock T is in this case predetermined by the clock signal TCK.

10　By way of example, Fig. 4 shows signal elements DIN[p] and DIN[n] which are associated with the data signal D on the two signal lines 20 and 30 when there are no faults; Fig. 5 shows the signal elements when, for example, there is one fault. This illustrates the situation if the signal line 30 is not

15　carrying a signal because of the fault.

In the example shown in Fig. 4 the two signal elements are phase-shifted through 180°, so that VP[1] = VN[0] and VP[0] = VN[1]. Furthermore, the magnitudes of each of the two signal

20　elements should be the same; therefore they should both each be centered about the mid-level.

As can be seen from Fig. 4, the mid-level signal M which is formed at the output 60 of the voltage divider 50 is always

25　the same when no faults are present while, in contrast, it changes its potential at the clock frequency when a fault is

present (see Fig. 5), to be precise from VP[1]/2 to VP[0]/2

and vice versa.

The potential change in now identified in the comparison

5   device 70 as shown in Fig. 2, as will be explained with

reference to Fig. 2. The edge-controlled toggle flip-flop 220

as shown in Fig. 2 operates as a frequency divider since its

two output signals Q and $\overline{Q}$ only ever switch on a falling edge

of the clock signal TCK. The output signals Q and $\overline{Q}$ on the

10   toggle flip-flop 220 are in this case inverted with respect to

one another, or are phase-shifted through 180° with respect to

one another. Therefore, the two sample and hold devices 200

and 210 operate in opposite senses. If – as already mentioned

above – a bit sequence which contains logic "zeros" and logic

15   "ones" alternately is now transmitted at the clock frequency

TCK via the data line 10 then the first sample and hold device

200 always, for example, samples the logic "ones" and the

second sample and hold device 210 in each case samples the

logic "zeros" specifically because each of the two sample and

20   hold devices 200 and 210 each detect only every alternate bit

since the toggle flip-flop 220 is operating at half the

frequency.

Thus, by way of example, the sample voltage or the sample

25   value for the mid-level signal M[1] for a logic "1" is

produced at the output A200 of the first sample and hold

device 200; the sample voltage or the sample value for the

mid-level signal M[0] in the case of a logic "0" is produced

by the second sample and hold device 210 at the output A210.

5   In this context, it shall be mentioned that it is irrelevant

to the operation of the apparatus 5 or to the operation of the

comparison circuit 70 whether the logic "1" is sampled by the

first or the second sample and hold device; furthermore, the

time sequence of the sampling of the logic "0" and "1" is not

10   important either.

In the comparison device 230, the difference voltage between

the two sample values or between the two sample voltages of

the two mid-values M is compared, for example by a comparator,

15   with a predetermined threshold value and the fault signal F is

produced if the discrepancy between the two sample voltages or

between the two sample values is greater than the

predetermined threshold value, that is to say if the

difference voltage between M[1] and M[0] is greater than the

20   predetermined threshold.

Fig. 3 shows an exemplary embodiment of a shift register cell

300 in which the signals F, SD and HSDIN which are produced by

the apparatus 5 shown in Fig. 1 can be buffer-stored for

25   further processing. The buffer-storage process is

particularly advantageous if the signals that are produced are

intended to be evaluated by analogous use of the "IEEE

Standard Test Access Port and Boundary-Scan Architecture"

cited above.

5 The memory register cell 300 has a first data input E300a, at

which the signal HSDIN can be fed in into the shift register

cell 300. The signal HSDIN can be used, for example, to store

whether the test sequence mentioned above and composed of

logic "zeros" and "ones" started with a logic "zero" or with a

10 logic "one".

The shift register cell 300 has a second data input E300b, at

which the fault signal F can be fed in. The output signal SD

from the Signal/Null-detect circuit 100 is fed in at the third

15 data input E300c.

In addition, the memory register cell 300 has connections

A300a and A300b, by which the illustrated memory register cell

300 can be connected to corresponding further cells.

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The contents of the memory register cell 300 can be erased via

a reset input R300. The memory register cell 300 is supplied

with a clock signal and a clock input T300.

25 Furthermore, the memory register cell 300 has a shift input

S300.

The input of the shift register cell 300 is formed by three multiplexers 310, 320 and 330 that are connected to the inputs E300a, E300b and E300c. Each of the multiplexers 310, 320 and

5　330 has a select input SEL; if a logic "0" is applied to the select input SEL, then the signal which is in each case applied in Fig. 3 to an input which is denoted under "0" (E310a, E320a, E330a) is passed on, to be precise to a respective downstream D flip-flop 350, 360 or 370. If, in

10　contrast, a logic "1" is applied to the shift input S300 and thus to the select inputs SEL of the multiplexers 310, 320 and 330, then the signal which is applied to the respective input (E310b, E320b, in E330b) annotated "1" in Fig. 3 is in each case passed to the respectively associated D flip-flop 350,

15　360 or 370.

Since the output of the D flip-flop 370 is connected to the input 320b of the multiplexer 320, and the output of the D flip-flop 360 is connected to the input E310b of the

20　multiplexer 310 and the output of the D flip-flop 350 is in turn connected to the input of a multiplexer which is no longer shown in Fig. 3, of a memory register cell which is no longer illustrated either, this effectively results in the data in the memory register cell 300 being "shifted up" along

25　the arrow direction indicated by arrow 400 when a logic "1" is applied to the shift signal S300.

Each of the D flip-flops 350, 360 and 370 is in each case

connected to the reset input, A300 and to the clock input

T300. All the D flip-flops 350, 360 and 370 can be erased via

5   the reset input A300; all the D flip-flops 350, 360 and 370

are clocked at the same clock frequency via the clock input

T300.